We claim:

1. A decoder comprising:

a plurality of N-parallel syndrome generators, each of the N-parallel syndrome generators coupled to a parallel data stream and being adapted to perform a calculation each cycle with N symbols from the parallel data stream;

a plurality of key equation determination devices, each key equation determination device coupled to at least one of the N-parallel generators and being adapted to determine at least one error polynomial; and

a plurality of N-parallel error determination and correcting devices, one for each of the N-parallel syndrome generators, each N-parallel error correction and determination device coupled to one of the key equation determination devices and being adapted to use the at least one error polynomial produced by the one key equation determination device to correct errors in the parallel data stream.

2. The decoder of claim 1, wherein N is three.

3. The decoder of claim 1, further comprising a device adapted to convert a serial input data stream into the parallel data stream.

4. The decoder of claim 1, wherein each symbol is a symbol from one of a plurality codewords from a frame, and wherein the decoder further comprises a device adapted to determine if a codeword is uncorrectable and adapted to output a number of uncorrectable codewords in the frame.

5. The decoder of claim 3, wherein:

the device creates a parallel data stream having a width of 48 symbols, wherein the device outputs 48 symbols every clock cycle;

N is three;

there are 16 three-parallel syndrome generators, four key equation determination devices, and 16 three-parallel error determination and detection devices, wherein each four of the three-parallel syndrome generators and three-parallel error determination and detection devices share one of the four key equation determination devices; and

the decoder outputs a second parallel data stream having a width of 48 symbols, wherein the decoder outputs 48 symbols per clock cycle.

6. The decoder of claim 1, wherein each symbol is a symbol from one of a plurality codewords in a frame, and wherein the decoder further comprises a device adapted to output a number of corrected bit errors per frame.

7. The decoder of claim 6, wherein the decoder further comprises a device adapted to disable error correction of the decoder when the number of corrected bit errors for each of a predetermined number of frames is less than a first predetermined value and adapted to disable the decoder when a deployed forward error correcting code cannot be processed by the decoder.

8. The decoder of claim 1, wherein:

each symbol is a symbol from one of a plurality of codewords;

the decoder further comprises a device adapted to output a second parallel data stream comprising corrected symbols; and

the decoder further comprises a device adapted to output a parallel stream of correction values, each bit in the parallel stream of correction values indicating a position in the second parallel data stream at which an error occurs.

9. The decoder of claim 8, further comprising a peripheral, the peripheral performing error analyses using the parallel stream of correction values.

10. The decoder of claim 1, wherein each key equation determination device further comprises a plurality of multiplication circuits, each of the plurality of multiplication circuits comprising a Mastrovito standard-basis multiplier.

11. The decoder of claim 10, wherein each Mastrovito standard-basis multiplier has a computation delay of (one DAND + five DXOR), where DAND denotes a delay of one AND gate and DXOR denotes a delay of one XOR gate.

12. The decoder of claim 10, wherein each N-parallel error determination and correcting device further comprises a division circuit, each division circuit comprising a composite-basis divider.

13. The decoder of claim 12, wherein each composite basis divider has a computation delay of (three DAND + nine DXOR), where DAND denotes a delay of one AND gate and DXOR denotes a delay of one XOR gate.

14. The decoder of claim 13, wherein each composite basis divider further comprises an inverter having a delay of (one DAND + three DXOR).

15. An encoder comprising:

a plurality of N-parallel encoders, each of the N-parallel encoders adapted to accept N symbol inputs, in parallel, during a cycle and produce, in parallel, N symbol outputs during a cycle, and wherein each N-parallel encoder is adapted to produce a plurality of redundancy symbols after a predetermined number of input symbols have been input to the encoder; and

a first device coupled to the N-parallel encoders and adapted to create an N-parallel frame, the N-parallel frame adapted to hold a plurality of codewords, each codeword comprising a plurality of symbols; and

a second device coupled to the N-parallel frame and adapted to create a serial data stream from a plurality of symbols in the N-parallel frame.

16. The encoder of claim 15, where N is three.

17. The encoder of claim 15, further comprising a third device adapted to create frame alignment information, the frame alignment information passed through one of the N-parallel encoders and placed at a beginning of the N-parallel frame.

18. The encoder of claim 15, further comprising a third device coupled to the second device and being adapted to create a parallel data stream having a width of 48 symbols, wherein the encoder outputs 48 symbols per clock cycle.

19. A method comprising the steps of:

converting a serial input data stream into a parallel data stream;

performing, in parallel, a plurality of N-parallel decodings of the parallel data stream to determine, in parallel, a plurality of error value and error locator polynomials;

correcting errors, by using a plurality of N-parallel correction and determination processes that use the error value and error locator polynomials, in the parallel data stream; and

outputting a second parallel data stream comprising a corrected version of the parallel data stream.

20. A system comprising:

a decoder comprising:

a plurality of N-parallel syndrome generators, each of the N-parallel syndrome generators coupled to a parallel input data stream and being adapted to perform a calculation each cycle with N symbols from the input parallel data stream;

a plurality of key equation determination devices, each key equation determination device coupled to at least one of the N-parallel generators and being adapted to determine at least one error polynomial; and

a plurality of N-parallel error determination and correcting devices, one for each of the N-parallel syndrome generators, each N-parallel error correction and determination device coupled to one of the key equation determination devices and being adapted to use the at least one error polynomial

produced by the one key equation determination device to correct errors in the parallel input data stream; and

an encoder coupled to the decoder and comprising:

a plurality of N-parallel encoders, each of the N-parallel encoders adapted to accept N symbol inputs, in parallel, during a cycle and produce, in parallel, N symbol outputs during a cycle, and wherein each N-parallel encoder is adapted to produce a plurality of redundancy symbols after a predetermined number of input symbols have been input to the encoder; and

a device coupled to the N-parallel encoders and adapted to create an N-parallel frame, the N-parallel frame adapted to hold a plurality of codewords, each codeword comprising a plurality of symbols.

21. The system of claim 20, wherein N is three, wherein the encoder is adapted to encode 40 gigabits per second (Gb/s), and wherein the decoder is adapted to decode 40 Gb/s.

22. The system of claim 20, wherein the system is part of a Synchronous Optical Network (SONET), wherein the decoder of the system is coupled to an optical receiver and the encoder is coupled to an optical transmitter, the optical receiver converting an optical data stream into a serial input data stream, the decoder further comprising a device adapted to convert the serial input data stream into the parallel input data stream, the encoder further comprising a device adapted to convert symbols from the N-parallel data stream to a serial output data stream that is coupled to the optical transmitter.

23. An integrated circuit comprising:

a plurality of N-parallel syndrome generators, each of the N-parallel syndrome generators coupled to a parallel data stream and being adapted to perform a calculation each cycle with N symbols from the parallel data stream;

a plurality of key equation determination devices, each key equation determination device coupled to at least one of the N-parallel generators and being adapted to determine at least one error polynomial; and

a plurality of N-parallel error determination and correcting devices, one for each of the N-parallel syndrome generators, each N-parallel error correction and determination device coupled to one of the key equation determination devices and being adapted to use the at least one error polynomial produced by the one key equation determination device to correct errors in the parallel data stream.

24. The integrate circuit of claim 23, further comprising:

a plurality of N-parallel encoders, each of the N-parallel encoders adapted to accept N symbol inputs, in parallel, during a cycle and produce, in parallel, N symbol outputs during a cycle, and wherein each N-parallel encoder is adapted to produce a plurality of redundancy symbols after a predetermined number of input symbols have been input to the encoder; and

a first device coupled to the N-parallel encoders and adapted to create an N-parallel frame, the N-parallel frame adapted to hold a plurality of codewords, each codeword comprising a plurality of symbols; and

a second device coupled to the N-parallel frame and adapted to create a serial data stream from a plurality of symbols in the N-parallel frame.